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AIR FORCE REPORT
SD TR-79-12
VOLUME I

LEVEL II

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GLOBAL POSITIONING SYSTEMS (GPS) HIGH DYNAMIC USER EQUIPMENT (HDUE) FINAL REPORT VOLUME I

(REFERENCE VOLUMES II AND III)

Prepared for:

DEPARTMENT OF THE AIR FORCE
Space and Missile Systems
Organization
Los Angeles, California 90009

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This final report was submitted by Texas Instruments Inc, Dallas, Texas, under Contract F04701-75-C-0180, with the Space and Missile Systems Organization, Air Force Systems Command, Los Angeles Air Force Station, Los Angeles, California.

This report has been reviewed by the Information Office (OIS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations. This technical report has been reviewed and is approved for publication.

JOSEPH A. STRADA, LCDR, USN
Director of Navigation Equipment & Avionics
Navstar Global Positioning System

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Summarizes Texas Instruments' efforts to design and develop an alternate High Dynamics User Equipment (HDUE) set for use during the Concept Validation Phase of GPS. Volume I summarizes design-to-cost objectives , production engineering program and reliability information obtained during field testing of HDUE 1 at Yuma Proving Ground., Yuma, Arizona, including failure data. Report documents Mean-Time-Between-Failure (MTBF) calculations. maintainability design considerations and suggested improvements for Phase II.

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SECTION I
INTRODUCTION

In June of 1975, Texas Instruments Incorporated was awarded Contract F04701-75-C-0180 to design and develop an alternate High Dynamic User Equipment (HDUE) set for use in the Concept Validation phase of the NAVSTAR Global Positioning System program. The contract and specification required a militarized system with maximum commonality and legacy to other classes of user equipment. Extensive performance testing, both in-plant and in the field, was also required.

This report is produced and submitted as Volumes I, II, and III of "The HDUE Final Reports" in accordance with Contract Data Requirements List (CDRL), Sequence Number A003. Volumes IV, V, and VI of the "The HDUE Final Reports" are defined as follows:

Volume IV	HDUE Legacy Report, SOW Para. 4.1.5
Volume V	HDUE In-Plant Test Report, CDRL Item No. A017
Volume VI	HDUE Field Test Report CDRL, Item No. A019

SECTION II
SET DESCRIPTION

This section is bound in Volumes II and III of this HDUE Final Report.

SECTION III
DESIGN TO COST

In order to optimize the GPS equipment with respect to cost, a Design-to-Cost (DTC) program was established in Phase I to provide a proper balance among cost, performance, and schedule. The major objectives were:

1. TI had the responsibility for developing and executing a plan of action to deliver equipment at or below price goals while continuously working to optimize development costs, production costs, life-cycle costs, equipment weight, reliability, performance, and maintainability. Phase I GPS equipment was designed and implemented with aggressive DTC plans directed towards future program savings.

2. The GPS program DTC process made use of the existing program organization by assigning DTC responsibility consistent with organizational constraints for the GPS system design and development. The TI DTC plan involved all levels of program management, design engineers, manufacturing engineers, integrated logistics support engineers, planning and control personnel, producibility personnel, production engineers plus various other TI support personnel. As an example of support personnel involvement, TI purchasing personnel encouraged our vendors to develop and maintain DTC programs.

TI was committed to an active and productive DTC effort throughout the GPS Phase I programs life-cycle and continued to develop cost savings within the constraints of future GPS business.

A. GPS DTC CYCLE

The DTC plan for GPS Phase I was submitted previously and contained the detailed DTC cycle flow which explained the various procedures TI used to incorporate DTC philosophy.

The drawings resulting from the hardware and system design were used to prepare cost estimates to establish the labor and material required to produce the equipment. Both project personnel and other groups contributed to the cost estimates which started with the lowest level part and built up through the top assemblies. The manufacturing engineers, purchasing personnel, producibility engineers, shop supervisors, assembly methods personnel and quality assurance engineers made independent assessments for the cost estimates based on their previous experience with the same or similar type equipment.

A DTC program took the current phase labor and material cost estimates and using various learning curves projected the cost in production quantities. The program provided direct labor and material costs and also added overhead, rework and other costs such as general and administrative costs and profit to determine the production unit price estimates.

The production cost estimates derived using the DTC program were compared to direct cost target budgets. If the estimated production costs were equal or less than the cost target budgets, further DTC actions were solicited in order to make further cost reductions. If the estimated production costs exceeded the cost target budgets, one or more of the following actions were taken.

1. DTC action items were identified revisions in system hardware design, test equipment, assembly methods, fabrication, test techniques, etc., which when incorporated, would reduce the

production cost without allowing the system performance or schedule to fall below minimum acceptable levels. Identification and incorporation of DTC action items were a continuous process throughout the life of the GPS Phase I program. Many revisions identified were very aggressive and were applied to future applications.

2. DTC reports were designed to keep TI design engineers, TI GPS Phase I program management, and SAMSO advised of the current DTC program cost status. The DTC processes were repeated or updated as required or as major impacts were discovered. This dynamic concept made it imperative that program personnel remained committed to an active and productive DTC effort throughout the GPS Phase I program life cycle.

B. GPS PHASE I DTC RESULTS

Specific DTC results from GPS Phase I DTC studies are numerous. Listed below are some of the major ones.

1. FPAU Integration

First Design	Second Design	Future Design
7 multi-layer boards	2 multi-layer boards	2 custom circuits
485 components	140 components	

2. Increased Capacity of Memory Modules

First Design	Second Design	Future Design
10 multi-layer boards	4 multi-layer boards	5 multi-layer boards boards
910 components	364 components	300 components

3. Frequency Synthesizer Changes

First Design	Future Design
2 multi-layer boards	1 multi-layer board
3 microwave amplifier	1 microwave amplifier
Analog switch	Digital oscillator

These examples illustrate the effective result of positive real cost savings demonstrated by the DTC effort on GPS Phase I program, after the design was proven during field testing.

SECTION IV
PRODUCIBILITY

Producibility engineers participated as integral members of the design production engineering team throughout the Phase I program. It was their responsibility to be intimately aware of the design and the plans of the engineers during the design effort and influence the design to the maximum extent possible to ensure that the product was built within the manufacturing operations of the Equipment Group so as to minimize total life-cycle costs. They were in the approval cycle of all drawings to verify their influence and to further ensure that a producible product was designed.

Producibility design guides were made available for particular areas of specialty to assist the design engineers in standardizing the design. The design guides had separate sections for fabrication, assembly, microwave integrated circuits, and printed circuit boards. Each listed the criteria, particularly suited for their shops, that would assist the shops in producing the product.

At an equal level of importance, performance was the criteria necessary to ensure the proper quality, reliability, and maintainability of the product during the Phase I design. These criteria were taken into consideration to ensure minimum cost.

Producibility engineers participated in other design considerations such as strength of material used, weight requirements, stress analysis, microelectronics circuitry and packaging, shop capabilities and capacity.

Specific examples of producibility studies in Phase I are: A "Common Module" approach was developed early in the Phase I program. A trade-off study was initiated to consider the effects of functional partitioning restraints, system costs, system packaging limitations, and user class environments on module size. Although the number of possibilities was infinite, several detailed parameters were listed as major considerations and addressed.

Two common module versions were used. One is housed in a shielded can while the other is an open card used for circuitry not requiring shielding or RF connections. All conform to MIL-STD-1389 dual span modules in width and center-to-center spacing and utilize standard extraction tools for removal purposes. Plans for module evolution included further reductions as further component integration occurred.

Secondly, a producibility study to determine the most cost-effective shielded can approach was performed on soldered on covers, three piece die castings, extrusions, and machined hog-out being the candidates. To meet Phase I cost and schedule goals the machined hog-out proved to be the best choice.

These examples are only a small portion of the producibility effort during the Phase I concept and validation phase in which Producibility Engineering was a vital part of the design team. The producibility objectives were achieved and GPS Phase I equipment is producible for the quantities and rates required in the Phase I contract.

SECTION V

RELIABILITY

This section documents the reliability information obtained while field testing HDUE 01 at Yuma Proving Grounds, Yuma, Arizona. Failure data from this testing is reviewed and discussed.

The reliability support effort for the High Dynamic User Equipment (HDUE) has been active since the early stages of proposal for contract. Reliability Engineering was responsible for the generation of a parts selection list and reliability design guide, including recommended component stress levels. After the design was complete, a data collection system was established to ensure good reliability growth during testing.

A. DESIGN EFFORT

1. Design Guide

During the design of the High Dynamic User Equipment, reliability was active in establishing specific guidelines, which were followed by the designing effort. One of the requirements of reliability was to write and deliver to the design engineers a Reliability Design Guide. The design guide consists of the following sections.

a. Derating Rules

Components reliability can be achieved only when the part does not receive stresses beyond those for which it was designed. In most cases, the lower the stresses placed on a component the more reliable it becomes.

The following derating rules define the maximum electrical stresses which the design engineer followed. These derating rules are part of Texas Instruments Standard Procedure 18-2. A copy of the derating rules is attached in Table 1.

b. Component Selection

The design guide also deals with the particular components and some of their characteristics:

- Resistors
- Capacitors
- Discrete Semiconductors
- Integrated Circuits
- Relays
- Switches
- Connectors
- Transformers and Inductors

In addition, each device catagory was broken down by specific component type, its applications discussed, and recommendations made for system use.

Table 1. Reliability Derating Rules

Part Type	Parameter to Derate	Derate to	Other Considerations
Diode	V_R	50%	
	I_O	50%	
	T_j 1/	120° C Max	
Diode, Zener	P_T	50%	
	T_j 1/	120° C Max	
Transistor	BV_{CEO} <20V	80%	
	20-50V	70%	
	50-120V	60%	
	> 120V	80%	Observe safe operating limits (SOA)
	T_j 1/	120° C Max	
IC, Digital	T_{pd} (54 TTL)	Add 40%	Add 0.15 nanosecond per pF additional load
	T_{pd} (Schotky TTL)	Add 20%	Add 0.15 nanosecond per pF additional load
IC, Linear	T_j	120° C Max	
Resistor, Fixed	Power	50%	Do not exceed maximum hotspot temperature, MIL-STD-199B
Resistor, Fixed, Metal Film (RNC)	Power	50%	50% of 70° C rating 80% of 125° C rating
Resistor, Variable	Power	50%	
Capacitor	DCWV	50%	DC bias voltage + AC peak not to exceed
	AC	50%	DCWV for all AC ratings

1/ It is not intended that the 120°C junction rule result in illogical design decisions on power semiconductors. Consult reliability engineering for tradeoff analysis and approval requirements for temperature exceeding 120°C

2. Preferred Parts List

In conjunction with the design guide, a preferred parts list was distributed to all engineers. The preferred parts list describes those parts whose use will best assure achievement of the contractual reliability obligations.

3. Parts and Drawing Review

During the design activity the responsibile project reliability engineer was included in the drawing review cycle. As the drawings were reviewed by the reliability engineer they were checked for proper documentation, use of established reliability components, contractual obligation and calculated component stress levels.

4. Stress Analysis

A worst case and normal operation stress analysis was performed on each printed wiring board, based on the circuit diagrams. From the stress data obtained, an analysis was performed in an effort to isolate components which were applied wrong or overstressed. If a problem was found, the reliability engineer recommended design changes and worked with the design engineer on the problem.

5. Reliability Prediction

Reliability Engineering conducted reliability predictions based on the High Dynamic design. These reliability predictions were initiated early in the design effort and were revised periodically to reflect changes in the design. This analysis was made by a failure rate build-up, in which a failure rate is assigned to each relevant piece part. The failure rates were obtained from MIL-HDBK-217B. TI and vendor historical failure data, engineering judgment and other sources were used for devices not covered in MIL-HDBK-217B. The part rates are summed to provide PWB level predictions; these rates, in turn, are summed to provide LRU and set level predictions. These calculations were performed by means of a TI developed computer program. "PLST," which automatically calculates failure rates and sums them, based on a computerized bill of materials, MIL-HDBK-217B, and environmental inputs. The above analysis resulted in a predicted failure rate expressed in units of "failure per million hours." This, in turn is inverted to yield a predicted MTBF in "hours." The final reliability prediction, which was calculated by PLST prior to system evaluation at Yuma, yielded an MTBF of 568 hours, well above the 500 hours specified.

B. TESTING SUPPORT

1. Board Level Testing

When a printed wiring board has completed assembly, the board is sent to Unit Test where a thorough examination of its electrical operation is performed. Should for any reason a board be found defective, the board is evaluated and the cause of the problem isolated. All defective components are removed and placed in an assembly and test reject part envelope ("Hold Bag"). All the necessary information for traceability of the defective part is written on the Hold Bag. The Hold Bag and component are then delivered to the reliability engineer. Records are kept along with the components to isolate failure trends.

2. System Testing

During testing of the High Dynamic User Equipment, a data collection system was used to locate and correct problem areas. The system used on the GPS Programs is titled the Reliability Failure Reporting

(RFR) system. Also, the Hold Bag is used to capture the bad components for record keeping and storage. This RFR system consists of a multicopy form, which keeps a complete history of a system failure down to the individual component failure analysis. The reliability engineer keeps an up-to-date record of all system failures with this form. Each form is prenumbered for easy record keeping and control. The number of the RFR is entered in the system paperwork at the time of a test failure. The RFR system has been used throughout the GPS program both inhouse and at the Yuma test grounds. A copy of an RFR form is attached as Figure 1.

C. FAILURE ANALYSIS

Table 2 lists all of the HDUE field failures in chronological order. This data was recorded on RFRs as described in subparagraph B-2. The symptom, analysis results, and any corrective action associated with each RFR are delineated.

D. SUMMARY

Texas Instruments is concerned about reliability and takes an active role in the development of a highly reliable system. Design and parts selection guides, which are individually tailored to this program, were published. These guides meet all the contract requirements, as well as design and reliability needs of the program. Guidelines such as parts control, stress deratings and preferred parts list clearly add to the overall reliability of the system.

Since field testing started, the performance of the High Dynamic System has been excellent. The number of failures which the system has experienced in the field is lower than that predicted. A total of 15 RFRs were presented in Table 2 above. These can be discussed in various categories.

PROJ. NO. | NO. 050801 | **RELIABILITY FAILURE REPORT (RFR)** | PROJ. NAME

SYSTEM/AC NO.	REJ. STA.	DATE	FAILED UNIT	SEQ/SER NO.	REF. DES.	OP. TIME

ORIGINATOR

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DESCRIPTION OF SYMPTOM

TEST PROCEDURE NO.	TEST PARAGRAPH NO.	ENVIRONMENTAL COND.	ORIGINATOR NAME

TROUBLESHOOTER

FAILED ASSEMBLY	SEQ. NO.	REF. DES.	PRODUCTION CONTROL	W.O./E.O. NUMBER

DESCRIPTION OF PROBLEM CAUSE AND REPAIR ACTION TAKEN

REJECTED PART DATA	PART NAME	PART NUMBER	PART REF. DES.	SERIAL NO.	DATE	TROUBLESHOOTER NAME

1. TROUBLESHOOT				2. REMOVE				3. REPAIR		4. REPLACE				5. ADJUST				6. FUNCTIONAL TEST			
SYS	WRA	SRA	MEN	WRA	SRA	S-SRA	MEN	ITEM	MEN	WRA	SRA	S-SRA	MEN	SYS	WRA	SRA	MEN	SYS	WRA	SRA	MEN
HR MIN	HR MIN	HR MIN	NO	HR MIN	HR MIN	HR MIN	NO	HR MIN	NO	HR MIN	HR MIN	HR MIN	NO	HR MIN	HR MIN	HR MIN	NO	HR MIN	HR MIN	HR MIN	NO

160

RELIABILITY

110

DATE Y M M D D	SYS/AC	REFERENCE DESIGNATOR WRA	SRA	S-SRA	SS-SRA	PART	WRA HRS	WRA SEQ/SER NO	SRA SEQ NO.	PART NUMBER	REJ STA	ENV	ADD RPT	RPT NO.

FAILURE ANALYSIS

130

PART D.C.	PART S/N	MFR. CODE	F.A. CODE	R.C.	FAILURE ANALYSIS RESULTS

PART D.C.	PART S/N	MFR. CODE	F.A. CODE	R.C.	FAILURE ANALYSIS RESULTS

DATE | EXAMINED BY

CORRECTIVE ACTION

CCA CAUSE AND CORRECTIVE ACTION

140

DATE | RELIABILITY

ADD INFO

ADDITIONAL INFORMATION

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DATA | RELIABILITY

TI-22085

Figure 1. Reliability Failure Report (RFR)

Table 2. HDUE 01 RFR List

Item No.	RFR No.	Relevant(R) Nonrelevant(N)	Date	Symptom	Analysis Results	Corrective Action
1	19429	R	03/21/78	5 VDC, improper regulation	LM109 K replaced	
2	47414	N	07/14/78	RCVR P.S. short	Transistor punch-through, elec. overstress; likely due to improper filter installation (Ref. 3)	Assembly/Manufacturing notified of problem
3	47417	N	07/14/78	Broken filter components, found in RCVR P.S, while incorporating an unrelated ECN	Mechanical overstress due to improper handling	Assembly/Manufacturing notified of problem
4	47416	N	07/27/78	RCVR P.S. short	4 transistors with C-B shorted and E open, due to excessive voltages; likely due to improper filter installation (Ref. 3)	Assembly/Manufacturing notified of problem
5	53185	N	07/31/78	No output from RCVR P.S.	3 ICs failed due to excessive voltages; likely caused by improper filter installation (Ref. 3)	Assembly/Manufacturing notified of problem
6	47460	N	08/02/78	Data errors	Design mod needed	Incorporated MI 2036169, Rev. A
7	47459	N	08/08/78	RCVR Code Gen Module, range Center unstable at start of operation	X1A-Code Generator IC replaced; in-house testing did detect problem	Implemented new test system; more comprehensive test is now done in-house

Table 2. HDUE 01 RFR List (Continued)

Item No.	RFR No.	Relevant(R) Nonrelevant(N)	Date	Symptom	Analysis Results	Corrective Action
8	47458	N	08/08/78	RCVR BIT indication no master time delay	X1-Code Generator IC, with intermittent short VCC to ground; transistor with shorted C-E, due to excessive VCE	
9	47453	N	08/24/78	Broken resistor found during unrelated inspection	Resistor broken	
10	47453	R	08/24/78	Intermittent contact between "RCVR" and "ERROR" positions of switch	Switch replaced	
11	47451	R	09/05/78	Weak narrowband board output	Mixer replaced	
12	47438	N	11/01/78	System failed to load compress tape correctly	MPM replaced, fixed problem, no failure found	
13	47448	R	11/04/78	Batteries dead on AC/DC Unit	Battery failed	
14	47449	R	11/04/78	Transistor and resistor bad on XA3 board	Transistor punch-through due to excessive VCE; resistor failure	
15	47447	N	11/15/78	System failed nav. DMM diagnostics	No failure found	

There were six RFRs that were not directly related to system functional operation:

- Items 2, 3, 4, 5 were all related to improper installation on one power supply
- Item 6 of Table 2 referred to incorporation of a Modification Instruction (MI)
- Item 9 was related to improper installation of a resistor

These were studied by the reliability engineer and communicated to the proper assembly/manufacturing personnel. No further events of this type have since occurred. Since these items did not affect actual system of operation, they were not considered relevant failures and were not included in MTBF calculations.

Item 7 resulted from an in-house unit test that was initially incapable of detecting certain minor flaws in the Code Generator Module. Since that time, a more elaborate test set has been devised and a more comprehensive unit test incorporated, so such problems can be detected early. This item was not considered relevant, because the actual problem occurred in-house and was not related to field operation of the equipment.

Two other RFRs (Items 12 and 15) referred to occurrences at which failures were indicated, but upon subsequent testing were found to be in good condition. These events are considered one-time operator errors, as they have not reoccurred. No corrective action is warranted at this time, and the events are not considered relevant failures.

The remainder of the failures, a quantity of six, are considered relevant, since they occurred during system operation and involved actual part failures. None of these failures has reoccurred and no trend is present. Corrective action, then, is limited to tracking future failures to assure no long-term trends are present, and to assure that the overall system reliability is within reasonable limits, achieving reliability growths with field operating time.

E. CONCLUSION

1. Mean-Time-Between Failure (MTBF) Calculation

The total of six relevant failures with 970 hours of field operations yields a cumulative MTBF of 162 hours. Typically, a new system can expect a reliability improvement from inital design to maturity that will increase MTBF by a factor of ten. If an MTBF growth of five to ten times is assumed for the mature HDUE, then an MTBF of 810 to 1,620 hours is projected. The MTBF prediction of 568 hours (reference subparagraph A-5) gives credibility to this projection.

2. Reliability Growth

The data summarized in Table 3 for HDUE 01 field testing indicates set reliability improvement over time. This is further substantiated by the fact that all of the RFRs, including those corresponding to relevant failures, occurred in the first 57 percent of the operating time.

Table 3. HDUE 01 Failure Summary

	1-2Q78	3Q78	4Q78	1Q79	2Q79	Total
Field Hours	270	170	140	240	150	970
RFRs	1	10	4	0	0	15
Relevant Failures	1	3	2	0	0	6

Duane's Postulate is used here as the basis for reliability growth planning. On other programs, TI has consistently achieved Duane Model growth rates of 0.4 to 0.5. If a growth rate of 0.4 and an MTBF of 162 hours at 970 operating hours are assumed, the set reliability is estimated to begin to exceed its 500 hour MTBF requirement after 13,870 hours of additional operation. Set reliability performance will be monitored closely in order to apply knowledge gained in this growth process to future designs.

B. MAINTAINABILITY DESIGN CONSIDERATIONS

1. Preventive Maintenance

There are no preventive maintenance requirements for the HDUE. All modules/printed circuit cards are replaceable without adjustment or calibration. There is a requirement to clean the Instrumentation Interface Unit (IIU) recording heads on a daily basis; however, such requirements will be eliminated on Phase II equipment.

2. Interchangeability

In consonance with DTC/LCC goals, a large percentage of printed circuit cards are directly interchangeable. This concept is an important contribution to maintainability requirements in that a suspect module may be interchanged with a like module for fault isolation. This is particularly significant in the receiver RF amplifer section.

3. Access

All system modules are easily accessed by removal of protective covers. With the exception of two modules, all SRUs can be quickly removed and replaced without removal of other SRUs. (See subparagraph C-1.)

4. Built-in Test/Performance Monitoring

Operational availability of the system is enhanced by software accessed performance monitoring capabilities. Operational software is used to the maximum extent in implementing the BIT function. The software approach largely eliminates hardware that is solely dedicated to the BIT function, eliminating the possibility that BIT hardware failures may be greater than the hardware being tested.

Three distinct test features have been incorporated in the system; the operator-initiated operational test, the processor self-test and the fault isolation test. A system fault is visually indicated to the operator via the Control Display Unit (CDU) front panel.

The operational test is initiated by the operator at power-up and complete system performance check is accomplished. If a fault is detected, the system will attempt to complete the performance check without additional operator activity. If a fault is not cleared, the fault and its location will be indicated by the CDU.

The processor self-test is a continuous software-controlled test following system initialization. Continuous performance monitoring using self-test features increases the confidence level that a mission can be completed without an undetected failure.

The fault isolation process is accomplished with diagnostic tapes and the Instrumentation Interface Unit (IIU). The CDU is utilized to command functional tests to fault isolate to the defective LRU or SRU.

C. SUGGESTED IMPROVEMENTS

1. Master Oscillator

Stabilization of the oscillator reaquires approximately eleven minutes. This time is detrimental to MCT because of the increased system checkout time following corrective maintenance. The oscillator meets contractual specifications, however, a reduction in stabilization time is a design goal for Phase II.

2. Power Supply Module and Antenna Switch (Receiver LRU)

These modules are located in the bottom of the receiver LRU and are not easily removed/replaced. Phase II design will alleviate these problems.

D. CONCLUSION

Design features of the HDUE, considering noted areas for improvement, ensure that ultimate maintainability requirements for future production will be attained. A program maintainability engineer will continue to monitor and evaluate design progress and to impose maintainability standards.

SECTION VII
SUMMARY

This HDUE Final Report has documented the technology, both hardware and software, and the philosophy that Texas Instruments implemented in their High Dynamic User Equipment for the GPS concept validation phase. The overall set as well as its individual modules has been explained. Texas Instruments HDUE concepts, techniques, and results of design-to-cost, producibility, reliability, and maintainability have been put forth as well.

This report, in conjunction with the Legacy, In-Plant Test, and Field Test reports, demonstrates that Texas Instruments has met and improved upon the letter and the spirit of Contract F04701-75-C-0180 with the HDUE development and testing.

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